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#14/Response 9/10/02 VS

PATENT
(5500-36101/TT2823CPA)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Gardner et al.
Serial No. 09/207,972
Filed: December 9, 1998
For: ULTRATHIN HIGH-K GATE DIELECTRIC WITH FAVORABLE INTERFACE PROPERTIES FOR IMPROVED SEMICONDUCTOR DEVICE PERFORMANCE

Group Art Unit: 2815
Examiner: Warren, M.

Atty. Dkt. No. 5500-36101

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August 23, 2002
Date

Kevin L. Daffer

AMENDMENT; RESPONSE TO OFFICE ACTION MAILED MAY 23, 2002

Box Non-Fee Amendment
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

This paper is submitted in response to the Office Action mailed May 23, 2002 to further highlight reasons why the application is in condition for allowance.

REMARKS

Claims 16-33 are pending in the case. Further examination and reconsideration of the presently claimed application is respectfully requested.

Section 103 Rejections:

Claims 16-19, 21, 23, 30, and 31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,320,238 to Kizilyalli et al. (hereinafter "Kizilyalli") in view of U.S. Patent No. 5,880,508 to Wu (hereinafter "Wu"). Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,596,214 to Endo (hereinafter "Endo") in view of Kizilyalli and Wu.

The Office Action states that "Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Endo (US 5,596,214)." (Office Action -- page 3). However, this rejection is explained with reference to Chou (U.S. Patent No. 5,994,734). The figure numbers and the reference numerals cited in the explanation match the description of Chou, not Endo. Therefore, it appears that the reference to Endo was made in error and that the rejection of claim 20 is over Chou not Endo. However, arguments as to the patentability of claim 20 over both Endo and Chou in view of the additional cited art are presented in this response to ensure that the rejection that the Examiner had intended to make is addressed. As will be set forth in more detail below, the § 103 rejections of claims 16-21, 23, 30, and 31 are respectfully traversed.

To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP § 2143.03. Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion or incentive to do so. *In re Bond,* 910 F. 2d 81, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). The cited art does not teach or suggest each and every element of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

The cited art does not teach or suggest a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor substrate. Claim 16 recites in part: "[a] semiconductor device, comprising: a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor substrate."

Kizilyalli discloses a gate stack structure having a dielectric material layer disposed on a substrate with a gate electrode disposed thereon. Kizilyalli, however, does not disclose a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor substrate. For example, Kizilyalli states that "oxidizable substrate 101 has disposed thereon a grown oxide layer with a silicon dioxide layer grown thereunder. The grown oxide layer and the oxide layer thereunder are shown generally at 102." (Kizilyalli -- col. 3, lines 15-18.) Kizilyalli also states:

> It is necessary to use an interface within the dielectric that acts as a stress cushion and a defect sink. In an exemplary embodiment of the invention, this layer may be the silicon dioxide layer (referenced herein as the stress-free oxide layer) grown underneath the first grown oxide layer by an oxidizing reaction at the interface. This oxide layer may be grown under near-equilibrium conditions and results in the traps being annealed out and a substantially planar, nearly stress-free silicon-silicon dioxide interface being formed by the newly grown silicon dioxide. (Kizilyalli -- col. 3, lines 48-58).

Therefore, although Kizilyalli discloses that growing a stress-free oxide layer under another previously grown oxide layer results in the traps being annealed out, none of the oxide layers disclosed by Kizilyalli contain nitrogen. Therefore, Kizilyalli does not teach or suggest a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor substrate, as recited in claim 16.

Wu discloses a MOSFET with a high permittivity gate dielectric. Wu, however, does not disclose a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor substrate. For example, Wu states that "an ultra thin silicon oxynitride layer 6 is formed on the top surface of the substrate 2." (Wu -- col. 2, lines 63-64.) Wu also states that "silicon oxynitride layer 6 is preferably deposited by thermal oxidation in N_2O or NO." (Wu -- col. 2, lines 65-66.) Wu, however, does not disclose that silicon oxynitride layer 6 is a low-trap-density oxide. Therefore, Wu does not teach or suggest a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor substrate, as recited in claim 16.

In addition, the combination of Kizilyalli and Wu does not teach, suggest, or provide motivation for a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor substrate, as recited in claim 16. For example, Kizilyalli teaches that a silicon dioxide layer must be thermally grown underneath other previously formed dielectric layers in order to anneal the traps in the dielectric layers. In this manner, if the silicon oxynitride layer of Wu is incorporated into Kizilyalli, Kizilyalli teaches that this silicon oxynitride layer must also be formed upon a thermally grown silicon dioxide layer, not on an upper surface of a semiconductor substrate. As such, the combination of Kizilyalli and Wu does not teach or suggest a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor substrate, as recited in claim 16.

The cited art also does not provide any motivation for eliminating or altering the composition of the stress-free thermally grown silicon dioxide layer of Kizilyalli formed under other dielectric layers and on an upper surface of oxidizable substrate 101. For example, Kizilyalli states that "what is needed is a dielectric structure, and its method of fabrication which enables...avoiding the problems of ultra-thin layers of silicon dioxide used in conventional structures." (Kizilyalli -- col. 2, lines 26-31.) Kizilyalli also states that "in developing thin dielectrics with low defect densities, not only is it necessary to reduce the initial defect densities, but also to reduce local stress-gradients near the silicon-silicon dioxide interface using a stress-accommodating layer." (Kizilyalli -- col. 3, lines 44-48.) As set forth above, the stress-accommodating layer is the silicon dioxide layer thermally grown underneath another silicon dioxide layer and on the upper surface of oxidizable substrate 101. In addition, Kizilyalli states that "the

high quality silicon-silicon dioxide interface results in a low interface trap density." (Kizilyalli -- col. 6, lines 52-53.) Therefore, eliminating or altering the composition of this stress-accommodating layer would render the gate stack structure of Kizilyalli being modified unsatisfactory for its intended purpose. For example, incorporating nitrogen into the stress-accommodating layer of Kizilyalli would render Kizilyalli being modified unsatisfactory for its intended purpose. If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984) MPEP 2143.01. Therefore, there is no suggestion or motivation to modify the stress-free silicon dioxide layer of Kizilyalli formed on an upper surface of oxidizable substrate 101 such that it contains nitrogen.

Furthermore, Kizilyalli states that "further details of the oxide growth layer at the Si-SiO_2 interface can be found in the following references: U.S. Pat. No. 4,851,370...incorporated specifically herein by reference." (Kizilyalli -- col. 3, line 59 - col. 4, line 3.) U.S. Patent No. 4,851,370 to Doklan et al. (hereinafter "Doklan") states that "the newly grown SiO_2 is structurally superior to the thermally grown and deposited oxides because the growth occurs under the stress accommodating conditions provided by the interface which acts as a stress cushion." (Doklan -- col. 5, lines 35-39.) Therefore, the stress-accommodating layer of Kizilyalli must be grown under two other existing dielectric layers having such a stress cushion. Wu, however, does not teach or suggest forming a dielectric layer under another dielectric layer previously formed on the substrate. Therefore, Wu cannot suggest modifying the formation of the stress-accommodating layer as taught by Kizilyalli such that this layer contains nitrogen.

Moreover, the cited art does not suggest the desirability of using a different layer or method to reduce the traps in the dielectric. For example, Doklan states that "the oxidation reaction during the densification anneal produces a reduction in the number of interface traps together with a simultaneous reduction in the interface stress gradient, roughness and number of asperities." (Doklan -- col. 5, lines 42-46.) Therefore, Kizilyalli, by incorporation of Doklan, teaches that it is the oxidation reaction that reduces the number of interface traps and reduces the interface stress gradient in the gate stack structure. Neither Kizilyalli nor Doklan, however, teach or suggest using any other reactions or forming any material other than silicon dioxide to reduce the interface traps or the stress gradient. In addition, Wu does not teach or suggest that the silicon oxynitride layer reduces the interface traps or the stress gradient. As such, neither Kizilyalli nor Wu suggests the desirability of modifying the stress-accommodating layer to include anything other than a silicon dioxide layer. The mere fact that references <u>can</u> be combined or modified does not render the resultant combination obvious unless the prior art also suggests the

desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Consequently, the combination of Kizilyalli and Wu does not teach, suggest, or provide motivation for the limitations of claim 16.

Endo also does not disclose a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor substrate, as recited in claim 16. For example, as set forth in more detail in a Response filed in this case on August 9, 2001, instead of describing a low-trap-density, Endo recites the need to increase the density of trap sites and further recites a method to increase the trap density. (Endo -- col. 21, line 44 - col. 22, line 46.) In addition, the non-volatile memory device taught by Endo appears to rely upon trap sites to operate correctly. (Endo -- col. 7, lines 14-20.) As such, Endo would be unsuitable for its intended purpose of maintaining captured electrons if modified to teach the claimed low-trap-density nitrogen-containing oxide. For at least these reasons, Endo teaches away from the presently claimed semiconductor device having a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor surface. Consequently, the combination of Endo, Kizilyalli, and Wu does not teach, suggest, or provide motivation for the limitations of claim 16. As a result, the combination of Endo, Kizilyalli, and Wu does not teach, suggest, or provide motivation for the limitations of claim 20, which depends from claim 16.

Chou discloses a modified gate structure for a non-volatile memory device. Although Chou appears to teach a first dielectric formed on a substrate (Chou -- col. 2, lines 59-60), Chou does not teach or suggest a semiconductor device having a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor surface, as recited in claim 16. Furthermore, Chou does not provide any motivation to modify the cited art such that their combination teaches the claimed low-trap-density nitrogen-containing oxide. Therefore, the combination of Chou, Kizilyalli, and Wu does not teach, suggest, or provide motivation for the limitations of claim 16. As a result, the combination of Chou, Kizilyalli, and Wu does not teach, suggest, or provide motivation for the limitations of claim 20, which depends from claim 16.

For at least the reasons cited above, claim 16 and claims dependent therefrom, are patentably distinct from the cited art. Accordingly, removal of the § 103 rejections of claim 16-21, 23, 30, and 31 is respectfully requested.

Allowable Subject Matter

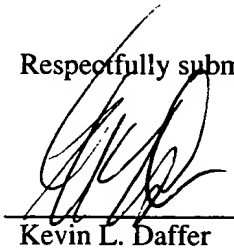
Claim 22 was objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 24-29, 32, and 33 are allowed. Applicant sincerely appreciates the Examiner's recognition of the patentable subject matter recited in claims 22, 24-29, 32, and 33. In addition to claims 22, 24-29, 32, and 33, Applicant believes the remaining pending claims are also allowable as set forth in more detail above.

CONCLUSION

In the present response, Applicants have responded to the objection to claim 22 and the rejections of claims 16-21, 23, 30, and 31. Accordingly, Applicants submit that this response constitutes a complete response to all issues raised in the Office Action mailed May 23, 2002. In view of the remarks traversing the rejections, Applicants assert that pending claims 16-33 are in condition for allowance. If the Examiner has any questions, comments or suggestions, the undersigned earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to Conley, Rose & Tayon, P.C. Deposit Account No. 50-1505/5500-36101.

Respectfully submitted,



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